REMARKS

In response to the Office Action dated June 8, 1995, claims are amended, claims are cancelled, and claims are added. Claims are now active in this application. Care has been exercised to avoid the introduction of new matter.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 2, 4, 5 and 9 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In support of this position, the Examiner identifies several words and/or phrases that are deemed confusing and/or lack clear antecedent basis. By this response, each of the noted points of indefiniteness has been appropriately addressed. Specifically, non-sequiturs are eliminated and confusing and/or vague language deleted in favor of language believed to recite the invention with the degree of precision and particularity required by the statute. Therefore, it is respectfully urged that the rejection be withdrawn.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

Claims 1-3, 12-14 and 31-33 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Kawai.

The Examiner contends that Adams "shows that failed address register (34) operate in synchronization with a clock signal (CL)."



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Claims 4 and 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Kawai and further in view of Getzlaff et al. and An.

Claim 9 stands rejected under 35 U.S.C. § 103 as being unpatentable over Ueoka in view of Kawai.

Kawai is relied upon to disclose a flip flop circuit where F/F, 201-208 function as a compressor for compressing ~~a~~ an output data of a circuit under test in synchronization with clock signals pulses and providing an output to a terminal. At column 2, lines 45-49 it is disclosed that the illustrated logic circuit uses the network 102 as a typical master/slave F/F network and causes a circuit to be tested, which brings the entire circuit shown in Fig. 1 into operation as a "synchronous sequential circuit". The Examiner implies that the circuit under test can be a memory array or arrays even though the background describes the invention relating to "a logic circuit for use in an arithmetic/logic unit in a computer."

Claim 10 stands rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Getzlaff.

Getzlaff is relied upon to disclose the use of a compressor having a first wired circuit having a plurality of n-channel FETs each having a gate receiving data read signals (C1, D1) and being connected in parallel to a first signal (GND), a second wired circuit having a p-channel FET, receiving read signals (B0, B1) and

being coupled in parallel to a second signal (VDD). The Examiner asserts that it would have been obvious to use the compressor of Getzlaff in place of the data compressor (32) of Adams in order to compress the data read from the memory cell array.

The rejections are respectfully traversed for the following reasons.

In discharging the initial burden of establishing a *prima facie* case of obviousness, the Examiner is obliged to explain precisely how and why one having ordinary skill in the art would have been led by the prior art as a whole to modify and/or to combine the applied prior art to arrive at the claimed invention. ***Uniroyal, Inc. v. Rudkin-Wiley Corp.***, *supra*. In establishing the requisite motivation, it has been consistently held that both the suggestion and the reasonable expectation of success must stem from the prior art itself, as a whole. ***In re Vaeck***, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); ***In re Fine***, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); ***In re Dow Chemical Co.***, 837 F.2d 469, 5 USPQ2d 1529 (Fed. Cir. 1988).

Applicant stresses that the requisite motivation to support the obviousness conclusion is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, ***In re Gyurik***, 596 F.2d

1012, 201 USPQ 552 (CCPA 1979). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. ***Carella v. Starlight Archery***, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); ***Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.***, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); ***ACS Hospital Systems, Inc. v. Montefiore Hospital***, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984); ***In re Ehrreich***, 590 F.2d 902, 200 USPQ 504 (CCPA 1979).

It is stressed also that the requisite motivation cannot be established by undercutting the expressed objectives of an applied reference. ***In re Fritch***, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992); ***In re Gordon***, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); ***In re Schulpen***, 390 F.2d 1009, 157 USPQ 52 (CCPA 1968). That is, the use disclosed in a secondary reference for an element to be included in the combination of a primary reference must be consistent with the objectives of the primary reference. The burden of establishing this consistency is on the Examiner as the initial burden of establishing a ***prima facie*** basis to deny patentability to a claimed invention is always upon the Examiner. ***In re Oetiker***, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992); ***In re Piasecki***, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

In the present invention, multi bit data, read out in parallel, is compressed into a one bit data as clearly recited in the claims ("compressing said data to one-bit data").

Adams compares a test pattern from a test pattern generator with a data patten read from a memory cell array and generates a one bit pass/fail signal based on the result of comparison, and stores an address signal from an address counter as a defective address in response to the pass/fail signal.

The Examiner maintains that the defective address register of Adams operates in response to a clock signal. However, the clock signal is the pass/fail signal (see column 3, lines 53-57) which is not generated in synchronization with a clock signal. The clock signal of the present invention provides the data output timing as well as operation timing of the memory device, and is substantially different from Adams' clock signal such as the pass/fail signal. Thus, Adams fails to disclose or suggest a read means for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command incorporated in synchronization with the clock signal.

Kawai discloses an arrangement for identifying whether a defect is present in a combinatorial logic network. Kawai arranges the master flip-flops 201-208 and the slave flip-flops 211-218 into circulating shift registers. A test pattern is initially set in the master shift register and in the slave shift register. The slave shift register functions as a random pattern generator whose output is sent into the combinatorial logic network. The master shift register receives and stores an output of the network.

Whether the network is defective is determined by observing whether the bit pattern stored in the master shift register is the same as that obtained when the network is normal.

Kawai describes at column 6, lines 61-63 that the master shift register operates as a compressor. However, the definition of "compress" in Kawai is substantially different from that in the present invention. In Kawai, when a defect is present in the network, the storage content in the master shift register is always different from an expected bit pattern in the subsequent clock cycles. Kawai performs the "compression" by comparing the bit pattern in the master shift register with a normal (expected) bit pattern in a certain clock cycle. In other words, Kawai compresses the clock cycles, and does not compress the bit pattern into one-bit data as required by the present claims. Kawai reads out the bit pattern stored in the master shift register for comparison with the expected bit pattern.

The Examiner asserts that Kawai's comparator (how compression is performed in Kawai) can be used in place of the compressor of Adam. However, Kawai's comparator, or the master shift register supplies a bit pattern in parallel and only compresses the clock cycles. Such arrangement cannot be combined with the arrangement of Adams. More precisely, Kawai processes a test pattern data and supplies a processed result in each clock cycle, which arrangement is peculiar to a logic circuit, and Kawai updates data in the

master shift register in each clock cycle. If the "compressor" of Kawai comprised of the master shift register is applied to the arrangement of Adams, the compressor of Kawai simple receives the memory cell data, and Adams' components such as a comparator for comparing the memory cell data store in Kawai's compressor with a test pattern and a pass/fail signal generator responsive to the comparator remain needed although the pass/fail signal may be generated in each clock cycle. It is believe that this clearly evinces indiscriminate combining of prior art references to arrive at the claimed invention which case law precedent admonishes should not be done.

Getzlaff discloses a set of submultiplexers for selecting a predetermined number of bits located beginning at an arbitrary position in consecutively arranged data bits. A multiplier includes an AND gate provided for each input, and an OR gate receiving outputs of AND gates. In accordance with an output of a multiplexer control, one AND gate is enabled on each submultiplexer and the output of the enabled AND gate is outputted through an OR gate.

In Getzlaff, only selection of a predetermined number of bits from a plurality of data bits is carried out, and no compression is carried out. Thus, contrary to the Examiner's assertion, there is no compressor in Getzlaff which can be used in place of the data compressor (32) of Adams in order to compress the data read from

the memory cell array.

It is believed that the present rejections evince a misunderstanding of the compressor of Kawai as well as the fact that there is no compressor in Getzlaff. More specifically, there are material differences between the claimed invention and the applied references, as well as between the elements of Kawai and Getzlaff which are to be combined with the arrangement of Adams.

It is submitted that it is clear legal error for the Examiner to fail to address differences between the claimed invention and the applied references in resolving the ultimate legal conclusion of obviousness under 35 U.S.C. §103 as required by ***Graham v. John Deere Co.***, *supra*. ***Bausch & Lomb, Inc., v. Barnes-Hind/Hydrocurve Inc.***, *supra*; ***Loctite Corp. v. Ultraseal, Ltd.***, *supra*; ***Jones v. Hardy***, *supra*.

Given the above described differences, it is Applicant's position that a conclusion of obviousness is not warranted as the Examiner has not articulated any logical reason why one having ordinary skill in the art would have been motivated to modify and/or combine the applied references to arrive at the claimed invention. Therefore, it is respectfully urged that the rejections of claims 1-5, 9, 10, 12-14 and 31-33 under 35 U.S.C. § 103 be withdrawn.

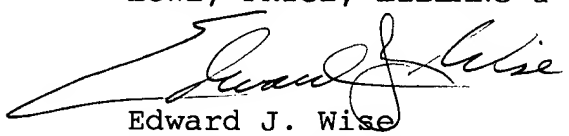
CONCLUSION

Accordingly, it is urged that the application, as now amended, overcomes the rejection of record and is in condition for allowance. Entry of the amendment and favorable reconsideration of this application, as amended, are respectfully requested. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 12-2237 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE, PRICE, LEBLANC & BECKER



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